In the Claims:

Please amend claims 1-15, and 17-23, as indicated below.

1. (Currently amended) A microprocessor, comprising:

an instruction cache;

a trace cache; and

a prefetch unit coupled to the instruction cache and the trace cache;

wherein the prefetch unit is configured to prefetch instruction code from a system
memory for storage within the instruction cache, wherein the system
memory is distinct from the instruction cache and the trace cache, wherein
the prefetch unit is further configured to prefetch a line of instructions
from the system memory into the instruction cache in response to a trace
being evicted from the trace cache, wherein the line of instructions is not
currently needed for execution, wherein the line of instructions prefetched
from the system memory is dependent on contents of the trace evicted
from the trace cache, and wherein the line of instructions is prefetched in
anticipation of instructions included in the evicted trace being re-executed.

2. (Currently amended) The microprocessor of claim 1, wherein the prefetch unit
is configured to prefetch a line into the instruction cache from the system memory
comprising instructions that correspond to operations that precede a branch in the evicted
trace.

3. (Currently amended) The microprocessor of claim 1, wherein the prefetch unit
is configured to prefetch a line into the instruction cache from the system memory

comprising instructions that correspond to operations that follow a branch in the evicted trace.

4. (Currently amended) The microprocessor of claim 1, wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache from the system memory in response to the trace being evicted from the trace cache.

5. (Currently amended) The microprocessor of claim 4, wherein the prefetch unit is configured to prefetch a number of lines from the system memory that is proportional to the number of branch operations comprised in the evicted trace.

6. (Currently amended) The microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache from the system memory in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache.

7. (Currently amended) The microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache from the system memory in response to the eviction of certain traces from the trace cache if the evicted trace is predicted unlikely to re-execute.

8. (Currently amended) A computer system, comprising:

a system memory; and

a microprocessor coupled to the system memory, comprising:

an instruction cache;

a trace cache; and

a prefetch unit coupled to the instruction cache and the trace cache;

wherein the prefetch unit is configured to prefetch instruction code from the
system memory for storage within the instruction cache, wherein the
system memory is distinct from the instruction cache and the trace cache,
wherein the prefetch unit is configured to prefetch a line of instructions
from the system memory into the instruction cache in response to a trace
being evicted from the trace cache, wherein the line of instructions is not
currently needed for execution, wherein the line of instructions prefetched
from the system memory is dependent on contents of the trace evicted
from the trace cache, and wherein the line of instructions is prefetched in
anticipation of instructions included in the evicted trace being re-executed.

9. (Currently amended) The computer system of claim 8, wherein the prefetch
unit is configured to prefetch a line into the instruction cache from the system memory
comprising instructions which correspond to operations that precede a branch in the
evicted trace.

10. (Currently amended) The computer system of claim 8, wherein the prefetch
unit is configured to prefetch a line into the instruction cache from the system memory
comprising instructions which correspond to operations that follow a branch in the
evicted trace.

11. (Currently amended) The computer system of claim 8, wherein the prefetch
unit is configured to prefetch a plurality of lines of instructions into the instruction cache
from the system memory in response to the trace being evicted from the trace cache.

12. (Currently amended) The computer system of claim 11, wherein the prefetch
unit is configured to prefetch a number of lines from the system memory that is
proportional to the number of branch operations comprised in the evicted trace.

13. (Currently amended) The computer system of claim 8, wherein the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache <u>from the system memory</u> in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache.

14. (Currently amended) The computer system of claim 8, wherein the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache <u>from the system memory</u> in response to the eviction of certain traces from the trace cache if the evicted trace is predicted unlikely to re-execute.

15. (Currently amended) A method, comprising:

evicting a trace from a trace cache; and

prefetching a line of instructions into an instruction cache from a system memory in response to said evicting;

<u>wherein the system memory is distinct from the instruction cache and the trace cache;</u>

<u>wherein the line of instructions prefetched from the system memory is dependent on contents of the trace evicted from the trace cache;</u>

wherein the line of instructions is not currently needed for execution, and wherein the line of instructions is prefetched in anticipation of instructions included in the evicted trace being re-executed.

16. (Original) The method of claim 15, further comprising checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace.

17. (Currently amended) The method of claim 16, further comprising inhibiting the prefetching of the line of instructions into the instruction cache from the system memory if the line of instructions is stored in the instruction cache.

18. (Currently amended) The method of claim 15, further comprising predicting the likelihood that the evicted trace will be re-executed and inhibiting said prefetching of the line of instructions into the instruction cache from the system memory if the evicted trace is predicted unlikely to re-execute.

19. (Currently amended) The method of claim 15, wherein said prefetching comprises prefetching a line into the instruction cache from the system memory comprising instructions that correspond to operations that precede a branch in the evicted trace.

20. (Currently amended) The method of claim 15, wherein said prefetching comprises prefetching a line into the instruction cache from the system memory comprising instructions that correspond to operations that follow a branch in the evicted trace.

21. (Currently amended) The method of claim 15, wherein said prefetching comprises prefetching a plurality of lines of instructions into the instruction cache from the system memory in response to the trace being evicted from the trace cache.

22. (Currently amended) The method of claim 15, wherein the number of lines prefetched from the system memory is proportional to the number of branch operations comprised in the evicted trace.

23. (Currently amended) A microprocessor, comprising:

means for evicting a trace from trace cache;

means for prefetching one or more lines into an instruction cache from a system memory in response to said evicting;

wherein the system memory is distinct from the instruction cache and the trace cache;

wherein the one or more lines of instructions prefetched from the system memory is dependent on contents of the trace evicted from the trace cache;

wherein the line of instructions is not currently needed for execution, and wherein the line of instructions is prefetched in anticipation of instructions included in the evicted trace being re-executed.